Nanoengineering Strategies for Metal–Insulator–Metal Electrostatic Nanocapacitors

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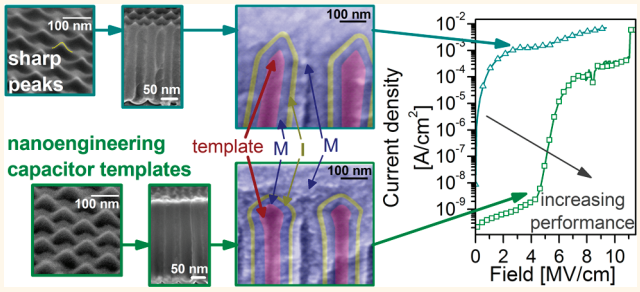
ABSTRACT



Nanostructures can improve the performance of electrical energy storage devices. Recently, metal–insulator–metal (MIM) electrostatic capacitors fabricated in a three-dimensional cylindrical nanotemplate of anodized aluminum oxide (AAO) porous film have shown profound increase in device capacitance (100× or more) over planar structures. However, inherent asperities at the top of the nanostructure template cause locally high field strengths and lead to low breakdown voltage. This severely limits the usable voltage, the associated energy density ($^1/_2CV^2$), and thus the operational charge–discharge window of the device. We describe an electrochemical technique, complementary to the self-assembled template pore formation process in the AAO film, that provides nanoengineered topographies with significantly reduced local electric field concentrations, enabling breakdown fields up to 2.5× higher (to >10 MV/cm) while reducing leakage current densities by 1 order of magnitude (to $\sim 10^{-10}$ A/cm^2). In addition, we consider and optimize the AAO template and nanopore dimensions, increasing the capacitance per planar unit area by another 20%. As a result, the MIM nanocapacitor devices achieve an energy density of ~1.5 Wh/kg—the highest reported.

KEYWORDS: energy storage · nanoengineering · metal–insulator–metal capacitor · anodic aluminum oxide · atomic layer deposition

The high surface areas of nanostructures are promising for achieving electrical energy storage devices with both higher energy densities and higher power densities than with conventional battery/capacitor configurations or microelectronic technologies.[1] Nanodevices that efficiently store larger amounts of energy *and* supply high bursts of power present significant application opportunities, including reduction of total system size and weight.[2] By offering access to thin layers of active storage materials through large surface areas, nanostructured devices can increase power for use of the energy capacity of the storage material. Where the energy is stored as surface charge on conducting electrodes (electrostatic capacitors) or in electrochemical double layers (ultracapacitor), the large surface area of nanostructures provides enhanced energy density per unit area, while power for such devices keeps surpassing significantly that of batteries and faradaic electrochemical capacitors.

Past work has shown that nanostructured designs of three-dimensional (3D) solid state metal–insulator–metal (MIM) electrostatic capacitors can achieve major advances in energy density (effective planar capacitance, EPC) compared to planar devices.[3–6] Recently, Bof Bufon *et al.* demonstrated a self-assembly technique for fabricating ultracompact capacitors with areal capacitance of up to ~200 μF/cm^2.[3] Beginning with a planar device (large footprint, relatively low-areal capacitance), the inherent differential mutlilayer stresses transformed the planar structure into a self-wound 3D ultracompact capacitor (reduced footprint, thus increased areal capacitance).[3] However, scaling to fill the remaining surface area with additional rolled-up capacitors seems a major challenge. Earlier, Banerjee *et al.* in our group demonstrated an EPC of ~100 μF/cm^2 with >10× increase in energy density for nanostructured electrostatic capacitors[5,6] by combining a 3D nanopore template of anodic aluminum oxide (AAO) with multilayer film deposition into the nanopores using atomic layer deposition (ALD).[7] AAO fabrication exploits natural, self-assembly during the

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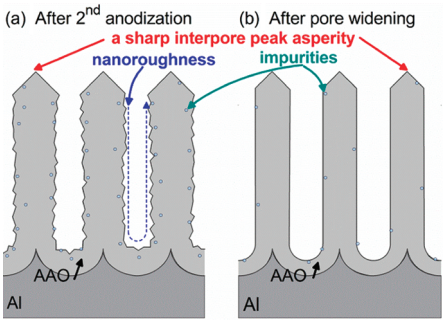

Figure 1. Schematic of AAO cross-section depicting the challenges of using AAO as a template for MIM capacitors. (a) Inherent interpore peak asperities cause premature breakdown, while nanoroughness of sidewalls and trapped impurities increase leakage current densities. (b.) Pore widening smoothes sidewalls removes impurities but does not blunt interpore peak asperities and does not reduce interpore asperities.

anodization process, resulting in a highly regular, highly ordered network of pores with high aspect ratios.[8] The self-limiting nature of ALD provides precise monolayer thickness control, which translates into exceptional conformality for inserting ultrathin multilayer coatings uniformly into the nanopores to form the MIM devices.[9,10]

While the nanostructured AAO template provides substantial area enhancement resulting in significantly higher effective planar capacitance densities compared to conventional planar thin film arrangements,[11−13] the associated AAO nanotopography introduces several technical challenges, depicted in Figure 1, that can substantially limit critical performance metrics. Nanoroughness and trapped impurities at the AAO sidewalls, resulting from the anodization process, can increase leakage current densities, thereby decreasing charge retention time.[5,6]

More dramatically, the self-assembly phenomenon that leads to nanopore ordering in AAO involves sharp asperities in the Al substrate surface, whose geometry is ultimately replicated between nanopores at the top of the AAO surface. When arrays of parallel storage nanodevices are formed over these asperities, they experience local high electric fields, leading to premature (low-field) electrical breakdown. This significantly restricts the maximum voltage and field usable for energy storage. The means to bypass these inherent defect sources are needed to develop viable energy nanotechnologies based on AAO templates.

Despite these considerations, nanostructured AAO-based MIM devices from our group[5,6] have shown dramatic increases in energy density (>10×), employing (1) AAO pore widening to remove impurity-contaminated regions and (2) deposition of an ALD passivation layer under the MIM structure to smooth the nanotopography.[14] While significantly reducing leakage current, these techniques did not avoid low-field breakdown at about 4 MV/cm, well below the 12 MV/cm breakdown field reported for Al_2O_3 dielectrics in DRAM structures.[6] Since the gravimetric energy density E of electrostatic capacitors is a strong function of voltage ($E = {}^1/_2CV^2$, where C is capacitance and V is applied voltage), significant increases in energy density can only be reached if the operating voltage window is extended well beyond the low-field breakdown regime caused by inherent asperities in the AAO nanotopography.

This paper considers key aspects of process optimization for AAO template formation, ALD layer parameters, and the resulting performance metrics for AAO-ALD-based electrostatic nanocapacitors, all important considerations in nanodevice design. We describe an electrochemical nanoengineering technique, complementary to the AAO fabrication process, that effectively tailors the nanotopography by transforming sharp interpore peak asperities into smooth, rounded peaks that diminish local electric fields. Microcapacitor devices are fabricated on these nanoengineered templates, each consisting of more than 5 million nanocapacitors wired together in parallel. As a result, the electrical performance is significantly improved, and we achieve energy densities of ~1.5 Wh/kg, about 2× that of our previous work.[6] Breakdown occurs at much higher fields, around 10 MV/cm or 2.5× higher than before, significantly increasing the operating voltage window and approaching intrinsic breakdown fields of the Al_2O_3 insulator. Finally, we assess the projected performance benefits that can be expected from this advance.

THEORY AND RESULTS

Geometric Modeling and Optimization of Nanocapacitors and Arrays. Here we address the design of the AAO template to maximize equivalent planar capacitance (EPC), that is, energy density per unit planar surface area, within the constraints of available electrochemical processes for AAO formation, nanopore modification, and embedding of typical MIM nanocapacitor layers within the nanopores (for additional details, see Supporting Information).

The AAO template consists of hexagonally ordered pores, spaced an equal distance apart called the interpore spacing (D_{int}), which determines the number of pores (or pore areal density, ρ).[15] It is generally accepted that D_{int} exhibits a linear relationship with anodization voltage, V_{anod}, such that D_{int} [nm] varies as 2.5 × V_{anod} [V].[16] AAO pore ordering occurs in discrete regimes which depend primarily on the electrolytic solution and V_{anod}. This poses a challenge in that not all regimes of pore density or interpore spacing are accessible. Commonly used anodization chemistries are as follows: sulfuric acid with V_{anod} between 19 and 25 V,[16−18] oxalic acid at 40 V,[8,16] and

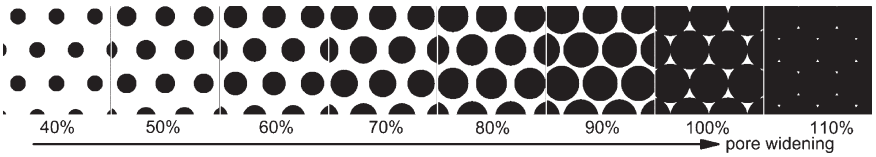

Figure 2. Schematic top-view of AAO template, where white regions indicate oxide and black regions indicate the pore openings. Pore widening increases the sidewall surface area, but widening beyond 100% degrades template integrity and stability.

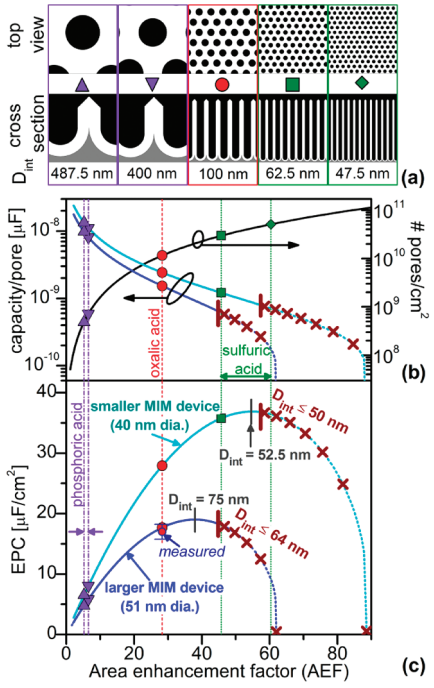

Figure 3. (a) Schematics of various anodization chemistries. Anodization voltages from left to right: 195, 160, 40, 25, and 19 V, where purple, red, and green symbols indicate phosphoric, oxalic, and sulfuric chemistries. (b) Increasing nanopore density (*i.e.*, reduced D_{int}) increases the area enhancement factor (AEF) but narrower pores reduce the capacity of each nanocapacitor. (c) Effective planar capacitance (EPC) for various anodization chemistries and AEFs for $L = 1\ \mu m$, $D_p = 0.8 \times D_{int}$, dielectric constant, $\kappa = 9$. The times symbols ($\times$) indicate where the specified finite MIM layers no longer fit within the pore diameters.

phosphoric acid between 160 and 195 V,[16,18,19] which we consider for determining the optimum EPC.

Once the nanopore template is established, pore widening techniques can be used to enlarge pore diameters independent of D_{int}. Figure 2 schematically represents increasing pore diameters for a given interpore spacing. To convey the message of this work, we simplify the discussion by choosing a restricted set of this parameter space. We use a design guideline that the pore diameter (D_p) should not exceed 0.8$\times$ the interpore spacing D_{int} and pore lengths (or AAO thicknesses, L) of 1 μm.

AAO template top-view and cross-section schematics for various anodization chemistries are shown in Figure 3a to illustrate how pore density influences the surface area available in the template. For deep pores with high aspect ratio AR (defined as pore depth/pore width), the presence of the pores dramatically increases the available surface area relative to that for a flat, planar surface. Accordingly we define area enhancement factor (AEF) as the total surface area (including pore sidewalls, pore bottom, and template top region between pores) per unit planar surface area (see Supporting Information). Figure 3a clearly shows that smaller interpore spacings results in greater pore densities and larger AEF.

Another set of device design parameters is the choice of thicknesses for metal, insulator, and metal layers of electrostatic MIM devices fabricated within the nanopores. Clearly, thinner dielectrics, and those with a higher dielectric constant increase capacitance, are subject to electrical performance concerns such as leakage current and low-field dielectric breakdown. In addition, metal layer thicknesses influence resistances that come into play in power metrics (*e.g.*, charge/discharge rates). Finally, fabrication process capability is very important since few approaches have the thickness control and conformality needed to produce ultrathin uniform layers inside very high aspect ratio nanopores. For our purposes here, we choose MIM device layer configurations based on Al−Zn-oxide (AZO)[20−22] as the conducting top electrode (TE) and bottom electrode (BE), with Al_2O_3 as the dielectric. We consider as examples two specific parameter sets, denoted by TE−dielectric−BE. One, referred to as the "larger MIM device" has a 51 nm diameter and is specifically a 10.5 nm AZO-8 nm Al_2O_3-7 nm AZO configuration, while the "smaller MIM device" has a 40 nm diameter and is 7 nm AZO-6 nm Al_2O_3-7 nm AZO. The choice of MIM layer thicknesses defines a minimum pore diameter required to accommodate the full MIM structure within the pore, although the resulting pore diameter may or may not be accessible by known chemistries for nanoporous AAO formation.

The capacitance for a device within a single nanopore (*i.e.*, an individual nanocapacitor) and the areal density of nanocapacitors (or nanopores) are plotted as a function of AEF in Figure 3b. For increasing AEF (*i.e.*, smaller D_{int}) the nanocapacitor areal density increases (right axis, Figure 3b). However, the capacity per nanocapacitor (left axis, Figure 3b) decreases with AEF, as higher AEF values imply smaller nanopore and MIM device diameters.

For high aspect ratio nanocapacitors the capacitance of each is dominated by the sidewalls, which is proportional to $1/(\ln(b/a))$, where b and a are the outside and inside diameter, respectively, of the dielectric layer separating the outer conducting layer (bottom electrode) from the inner conducting electrode (top electrode) (see Supporting Information). The ratio of these radii varies as function of active layer thicknesses, consistent with pore diameters, and two generalities can be made.

First, for a given MIM device layer structure, wider pores have a higher capacity per nanocapacitor, thus preferring phosphoric > oxalic > sulfuric. For example, for the larger MIM device within a phosphoric acid template (pore radius, R = 160 nm, b = 149.5 nm, and a = 141.5 nm) b/a is ~1.05. For the same layer structure within an oxalic acid template (R = 40 nm, b = 29.5 nm, and a = 21.5 nm) b/a is ~1.37. Since capacitance is related to the inverse of the b to a ratio, the same layer structure in a wider pore (R = 160 nm) yields higher capacitance than in a narrower pore (R = 40 nm). Similarly, the smaller MIM device shows decreasing capacitance per nanocapacitor as the pore diameter narrows.

A second observation from Figure 3b is that for a given template, a thinner bottom electrode ($t_{be} = R - b$) as well as thinner insulators ($t_{ins} = b - a$) provide higher capacitance (assuming the top electrode fills the remaining portion of the pore). Comparing the two device layer structures within an oxalic acid pore (R = 40 nm), the larger MIM device (b = 29.5 nm, a = 21.5 nm, $b/a \approx 1.37$) has a lower capacitance than does the smaller MIM device (b = 33 nm, a = 27 nm, $b/a \approx 1.22$). As in a parallel plate capacitor, decreasing the t_{ins} increases the device capacitance. However, unlike a parallel plate capacitor, the value of t_{be} in a porous nanocapacitor influences the capacity since this determines b. Thus, a thinner bottom electrode shifts b and a to larger values, which results in smaller b/a and higher capacitance.

An important consideration is the design constraint that the MIM device must fit within the pore diameter, which in turn is constrained by the mechanical stability of the AAO template (*e.g.*, as suggested in the guideline that $D_p \leq 0.8D_{int}$). This limits the usable AEF to ~45 and ~57 for the two examples considered, a feature which is depicted in Figure 3b by the vertical bars at these values and the times symbols (×) at higher AEF values, indicating that the device is no longer able to fit within the constraints of the template. For the larger MIM device the 51 nm diameter fully fills the pore diameter when $D_{int} \approx 64$ nm (at AEF ≈ 45), while the smaller MIM device's small diameter (40 nm) enables its use at higher AEF values corresponding to $D_{int} \approx 50$ nm (at AEF ≈ 57).

Device and Template Optimization. Given that a very large number of nanocapacitors will be wired together in parallel for use as a storage device, the capacitance per unit planar area is shown in Figure 3c as the equivalent planar capacitance (EPC). EPC depends on the product of areal density of MIM devices (or nanopores) and the capacitance per device, which respectively increase and decrease with AEF (Figure 3b). Accordingly the theoretical EPC first increases with AEF, then decreases at higher AEF, as shown by the smooth curves in Figure 3c. For the larger and smaller MIM device examples shown, EPC maxima occur in the range of AEF = 35−50, somewhat before the MIM size constraint (to fit into the nanopore) takes over (again shown by vertical bars and times symbols (×) in Figure 3c). This modeling is validated by experiment, illustrated by an experimental EPC ("measured") value for an oxalic acid template shown in Figure 3c, in good agreement with the model.

As seen in Figure 3c, the model suggests that, on net, larger EPC values are achieved with smaller pores and MIM devices within them. Within the suggested design guidelines, sulfuric and oxalic acid templates provide significant EPC gain compared to phosphoric. While the benefit of sulfuric over oxalic is notable, the thinner layers required pose more challenging process control constraints. The maximum EPC for the larger MIM device occurs near D_{int} = 75 nm compared to D_{int} = 52.5 nm for the smaller MIM device. The benefit of moving from the larger MIM device (51 nm diameter) to the smaller MIM device (40 nm diameter) is greater for oxalic as compared to phosphoric templates, increasing EPC by ~60% for oxalic compared to only by ~20% for phosphoric.

These results demonstrate that the realistic imposition of finite-size MIM devices within the nanopore templates adds geometric constraints to the optimization problem. Optimized templates for reaching near-maximum EPC must consider the density of nanocapacitors, their detailed geometric specifications and material properties, and the precision with which the designs can be realized on a massive integration scale.

While thinner active layers are beneficial for increasing EPC, this may introduce limitations on other critical performance metrics. For example, the dielectric must be thick enough to avoid excessive leakage current from Fowler−Nordheim tunneling, direct tunneling, and leakage or low-field breakdown associated with defects. Additionally, the electrode must be thick enough to achieve sufficiently low series resistance. Electrodes that are very thin may have low conductivity,[23] which would increase the RC time constant, limiting the capacitor's ability to rapidly charge and discharge for providing high bursts of power.

For the experimental component of this work, we selected oxalic acid templates as the MIM capacitor platform because these yield substantially higher EPC as compared to planar devices and provide adequate space for depositing adequate MIM layer thicknesses

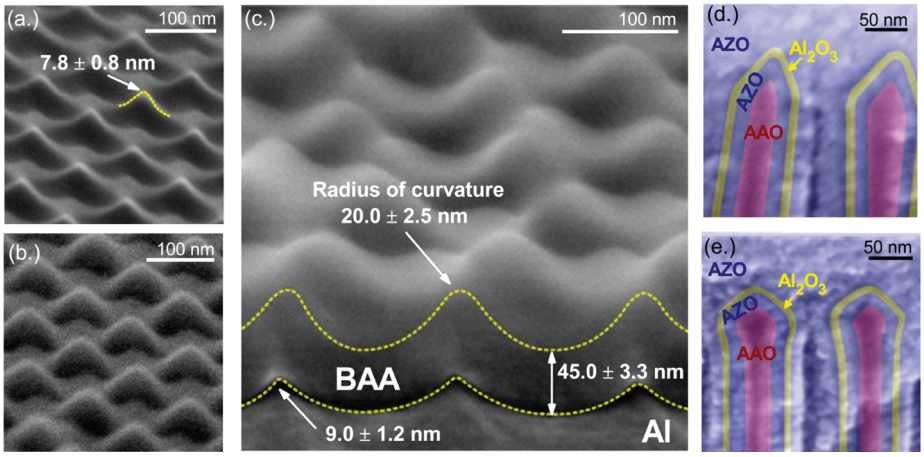

Figure 4. (a) SEM image of first anodized Al surface shows scalloped texture. (b) Formation of a BAA layer (40 V) on the first anodized surface smoothes scallop asperities. (c) Cross-section of the BAA shows the radius of curvature above and below the BAA layer. (d) Cross-sectonal SEM for MIM capacitor fabricated without BAA intermediate step, resulting in sharp interpore asperities. (e) SEM for MIM capacitor fabricated with BAA intermediate step, resulting in rounded interpore peaks.

along with a passivation layer. The remainder of this paper describes the experimental method of nanoengineering the oxalic acid template topography and the significant effect this has for reducing leakage currents and increasing breakdown fields.

Smoothing Template Nanotopography. Fabricating a highly uniform, ordered porous AAO template is typically achieved with a two-step anodization process.[8] After the first anodization the porous oxide is removed, leaving a scalloped texture on the Al surface as shown in Figure 4a. This pattern is essential for creating the ordered porous structure during the subsequent second anodization. However, the sharp peaks in the Al surface have a small radius of curvature (7.8 ± 0.8 nm) which directly produce corresponding sharp interpore peak asperities upon growth of the final AAO template during the second anodization step (Figure 1).

Before forming the final nanopore AAO template by the normal second anodization, we carried out an intermediate electrochemical anodization process in neutral solution to form a nonporous oxide film, referred to as barrier anodic alumina (BAA). Figure 4b shows the results of this intermediate processing step, which transforms the sharp peaks into smoother nanoengineered domes without degrading the ordering of the dimpled texture required for pore ordering during the second anodization. A higher resolution cross-sectional SEM image of this BAA layer on the scalloped Al surface, shown in Figure 4c, indicates the radius of curvature at the top of the BAA layer is significantly increased to 20.0 ± 2.5 nm from 9.0 ± 1.2 nm at the BAA/Al interface, with a BAA film thickness of 45.0 ± 3.3 nm at the dimple minima. Even though the peaks at the BAA-Al interface (Figure 4c) have a radius of curvature (9.0 nm) only slightly larger than that (7.8 nm) of the peaks on the Al scalloped BAA-free surface (Figure 4a), the rounded nanotopography (radius of curvature 20.0 nm) of the BAA top surface (Figure 4c) is retained during subsequent second anodization to form the final AAO nanopore template.

Cross-sectional SEM images show MIM nanocapacitors fabricated on an AAO template following a normal two-step anodization process without an intermediate BAA step (Figure 4d) and with an intermediate BAA step (Figure 4e). With transparent colors overlaying the SEM cross-section images to guide the eye, it is clear that the curvatures are less sharp at the interpore peaks because of the BAA step (Figure 4e). MIM layers (AZO−Al_2O_3−AZO) on the normal two-step anodized BAA-free template appear to be stretching over sharp peak asperities (Figure 4d), while the MIM layers appear to have much gentler bending when built on a BAA-AAO template (Figure 4e).

Electrical Consequences of BAA Smoothing Layer. To evaluate resulting electrical properties, we deposited MIM layers within AAO templates with varying BAA voltage and pore depth. Actual thicknesses are very near the targeted thicknesses: 10.2 ± 1.0 nm Al-doped ZnO (AZO) bottom electrode and 7.3 ± 0.9 nm of Al_2O_3 insulator. Unlike past work which used TiN as the electrode material,[6] this work used AZO to explore broader conducting layers and to determine if this material system is suitable to transparent optical devices.

Figure 5a shows representative current−voltage (IV) curves of selected devices. Electrode series resistance was measured with an additional IV sweep after catastrophic failure that caused shorting of the MIM capacitors. Reported electric fields have been adjusted to compensate for series resistance in order to accurately determine the actual breakdown fields and leakage currents. Even though AZO film resistivity is low as measured in planar thin films,[20] it was expected the thin-film 3D nanoelectrodes would introduce consequential resistance (~10 kΩ). These measured

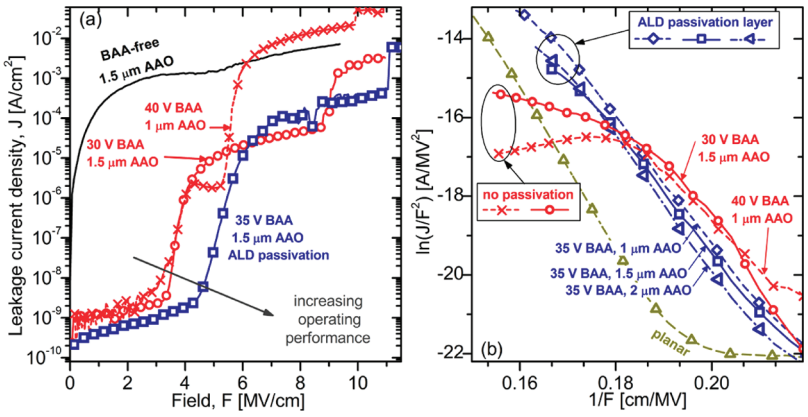

Figure 5. (a) Representative IV curves for AZO−Al_2O_3−AZO capacitors fabricated in AAO templates showing influence of BAA smoothing layer and ALD TiN passivation layer. (b) Linear segment indicate FN tunneling regime, which occurs for wider ranges and higher fields with the introduction of an ALD TiN passivation layer.

values are in good agreement with the expected resistance of thin-film AZO.

The nanoengineered templates show dramatic electrical performance improvements. Devices on the BAA-free 1.5 μm thick AAO (representative sample shown in Figure 5a) has very high leakage current densities at low fields (>10^{-4} A/cm^2). Devices built on nanoengineered templates using the BAA smoothing step, including 1 μm thick AAO with BAA formed at 40 V, and 1.5 μm thick AAO with BAA formed at 10, 20, 30, and 40 V (referred to in text as 40BAA-1 μm, 10BAA-1.5 μm, 20BAA-1.5 μm, 30BAA-1.5 μm, and 40BAA-1.5 μm, respectively), all showed similar dramatic reduction of leakage current, illustrated by the 40BAA-1 μm and 30BAA-1.5 μm IV curves in Figure 5a. Leakage currents are reduced by $10^5\times$ for all templates by a BAA intermediate processing step. At 1 MV/cm field, leakage currents are on the order of 10^{-9} A/cm^2. Increasing AAO template thickness from 1 to 1.5 μm did not change leakage currents.

Additionally, significant increases in breakdown fields were observed from nanoengineered templates that included the BAA layer, including breakdown fields of 9.0 $\pm$ 1.4 MV/cm for 10BAA-1.5 μm, 9.6 $\pm$ 0.8 MV/cm for 20BAA-1.5 μm, 9.5 $\pm$ 0.8 MV/cm for 30BAA-1.5 μm, and 9.5 $\pm$ 0.7 MV/cm for 40BAA-1.5 μm. Breakdown fields for 40BAA-1 μm (9.5 $\pm$ 1.5 MV/cm) are nearly identical to 40BAA-1.5 μm, indicating breakdown fields are also independent of AAO thickness.

These results demonstrate major improvements in leakage current and breakdown field due to the BAA smoothing layer. We attribute the improved breakdown characteristics to rounding of the interpore asperities inherent in AAO templating and the lower leakage current to the lower fields present (hence lower Fowler−Nordheim currents at asperities).

ALD Passivation Layers to Suppress Impurity Diffusion. Electrical performance was further improved by introducing a thin titanium nitride (TiN) ALD passivation layer prior to MIM layer deposition.[24,25] All samples with a passivation layer were fabricated using AAO thicknesses of 1, 1.5, and 2 μm with BAA formed at 35 V (referred to as 35BAA-1 μm-p, 35BAA-1.5 μm-p, and 35BAA-2 μm-p in the text, respectively). Of the samples with a passivation layer, for clarity, only 35BAA-1.5 μm-p is shown on Figure 5a. Low-field leakage current densities at 1 MV/cm were substantially further reduced from about 1.13 $\times$ 10^{-9} A/cm^2 to 4.7 $\times$ 10^{-10} A/cm^2 for 35BAA-1 μm-p, 4.6 $\times$ 10^{-10} A/cm^2 for 35BAA-1.5 μm-p, and 4.3 $\times$ 10^{-10} A/cm^2 for 35BAA-2 μm-p. In addition, breakdown fields were also further increased to 10.2 $\pm$ 1.5 MV/cm for 35BAA-1 μm-p, 35BAA-1.5 μm-p, and 35BAA-2 μm-p (see Supporting Information). More importantly, these fields are well within the range of theoretical and experimental breakdown fields of Al_2O_3.[26−28] These results suggest that the passivation layer suppresses diffusion of impurities from the AAO surface into the MIM device, improving leakage current and breakdown field, and confirming that 3D nanotemplates, initially intended to increase capacitance densities, have been effectively nanoengineered to meet critical electrical performance metrics. The nanoengineered template no longer introduces an intrinsic mechanism for low-field catastrophic failure, and allows significantly higher operating electric fields (near the strength of the insulator) to be used, with accompanying benefit to energy density $^1/_2CV^2$.

Leakage currents in MIM structures are typically dominated by electron tunneling over a barrier, that is, Fowler−Nordheim (FN) tunneling. FN analysis of current−voltage behavior is shown in Figure 5b for AZO−Al_2O_3−AZO MIM nanocapacitor devices with BAA layers and ALD TiN passivation, in comparison to corresponding planar MIM on a SiO_2 wafer. These curves exhibit a classic FN-tunneling regime governed by $J = AF^2\exp(B/F)$, where J is the leakage current density, F is the applied field, and A and B are constants.[29] The linear region indicates the regime where FN-tunneling dominates charge transport across the capacitor dielectric. 40BAA-1 μm and 30BAA-1 μm display FN tunneling over a narrow range,

0.20 to 0.22 cm/MV in Figure 5b, from which a barrier height of *ca.* 1.3−1.4 eV is derived. 35BAA-1 μm-p, 35BAA-1.5 μm-p, 35BAA-2 μm-p, and the planar device show characteristic FN-tunneling over a broader range in Figure 5b, 0.16−0.21 cm/MV and an increased barrier height of ∼1.8 eV.

Unexpected IV behavior is observed for 40BAA-1 μm between ∼4 and 6 MV/cm in Figure 5a, where the slope is no longer positive, suggesting negative resistance. Although the representative IV curve for 30BAA-1.5 μm does not display uncharacteristic behavior, many devices on this sample (and on many devices on 10BAA-1.5 μm, 20BAA-1.5 μm, and 40BAA-1.5 μm samples) showed uncharacteristic behavior in this range. One possible explanation is that these templates involve a dominating, counter-acting leakage mechanism to conventional FN tunneling, which could result from foreign ionic species as impurities. During anodization for oxide formation, electrolytic solutions dissociate, negatively charged ions move toward the oxide−Al interface, and positively charged ions move toward the oxide−electrolyte interface, both likely remaining trapped in the oxide membrane.[30−32] Under an electric field, these ions could become mobile and enter active layers, possibly causing this anomalous behavior. The introduction of a TiN passivation layer, like the Al_2O_3 example noted previously,[5,6] seems to diminish or eliminate the uncharacteristic behavior, suggesting the role of these layers as diffusion barriers that prevent migration of impurities from the AAO material into the nanodevice.

Capacitance measurements of all devices were in good agreement with the theoretical estimates provided by the geometrical calculations. The EPC of 11.6 ± 0.5 μF/cm^2 for 35BAA-1 μm-p, 20.6 ± 0.4 μF/cm^2 for 35BAA-1.5 μm-p, and 26.2 ± 1.5 μF/cm^2 for 35BAA-2 μm-p scales with increasing AAO template thickness (or pore depth). Comparing these EPC values with those reported by Banerjee *et al.* for thicker AAO templates,[6] we observe and project a ∼20% increase in EPC per unit AAO thickness. The IV curves (Figure 5a) show that nanotopography smoothing of interpore peak asperities by BAA−AAO is highly effective for nanoengineering the topography and increasing energy density. This BAA−AAO technique combined with a thin 4 nm TiN passivation layer (compared to thicker, 15 nm of Al_2O_3[6]), adds to the performance improvement by providing more space within the template, and resulting in larger AEF and EPC (refer to Figure 3). As a result, a projection of the EPC for devices fabricated on thicker AAO templates shows that significantly higher EPC should be attainable with greater AAO thicknesses.

DISCUSSION

The results described above illustrate the importance of detailed nanoengineering of energy storage nanostructures, and the challenges involved. Taken together, the 20% increase in EPC per unit AAO thickness and 2.5× improvement in breakdown field (6.25× increase in energy density $^1/_2CV^2$) suggest a total areal energy density increase by a factor of 7.5×. As compared to Banerjee *et al.*,[6] the devices characterized in this work had a much thinner passivation layer, which resulted in greater values of *b* and *a* (see Supporting Information). Assuming material densities of 5.62 g/cm^3 for ZnO,[21] 3.0 g/cm^3 for Al_2O_3,[33] and 3.0 g/cm^3 for TiN,[34] the active material mass per nanocapacitor is increased by a factor of about 3.7×. Therefore, the experimental parameters used here result in larger mass, reducing the energy density increase expected from 7.5× to about 2×. Nevertheless this represents a significant increase in energy density from 0.7 Wh/kg in previous work[6] to 1.5 Wh/kg.

Further improvements in electrostatic nanocapacitor performance can be foreseen. Some of these reside in the materials aspects of the design. The use of high-κ dielectrics (*cf.* Al_2O_3) offers benefits in energy storage density (linear in κ), but can encounter problems with leakage current and breakdown field.[27] Engineered nanomaterials can address some of these challenges, for example, by introducing Al dopant into high-κ ALD TiO_2.[35] Lower resistivity, ultrathin electrodes can be achieved by ALD, illustrated by the example of Ru,[36] which has potential to reduce series resistance by ∼10^3× compared to the AZO employed here.

Another source of opportunity lies in modeling and optimization of the MIM structure itself for electrical performance. While the examples considered in Figure 3 assumed a specific set of layer thicknesses, these parameters may be varied and optimized as well, leading to a broader picture than Figure 3. The geometry as well as the resistivity of the metal electrodes will affect power capability of the electrostatic nanocapacitor, functioning as a distributed resistance network whose power handling capability is improved by thicker, shorter nanoelectrodes. If higher κ dielectrics are employed, or larger area enhancement factor geometries used, leakage currents will likely increase, degrading the retention time during which the energy is stored for transfer to other circuitry. Modeling and optimization of the active device, its impact on overall performance in AAO template geometries, and the associated charge, retention, and discharge dynamics are beyond the scope of this paper but will be the focus of future publications.

CONCLUSION

Detailed nanoengineering of AAO-ALD electrostatic MIM nanocapacitors has enabled significant performance improvements. By electrochemically shaping and smoothing AAO nanotopography using an intermediate BAA smoothing layer, breakdown fields for

MIM layers over this topography have increased by 2.5×, from about 4 MV/cm to about 10 MV/cm (approaching intrinsic dielectric strength of the Al_2O_3 insulator), with benefit to energy density that scales with V^2. In general, devices based on self-assembly techniques are likely to offer a more affordable solution, but without nanoengineering techniques, like BAA, the notion of replacing traditional expensive templating techniques would not be feasible, since cost is not necessarily an equal trade-off to performance. AAO template nanoengineering combined with a thin metallic material is as effective at passivating ions as a thick dielectric material used by Banerjee *et al.*[6] An ultrathin TiN passivation layer under the MIM structure reduces leakage current densities to the 10^{-10} A/cm^2 range, serving as a diffusion barrier to prevent impurities from the AAO material entering the active MIM structure. Modeling and optimization of the template geometry increases capacitance density by 20% due to more efficient utilization of nanopore volume. As a result of these improvements, expected energy densities are 1.5 Wh/kg, the highest ever reported for electrostatic MIM nanocapacitors and 2× that of our previous work.[6] This work also illustrates the numerous factors of device design, materials choice, process engineering, and multiparameter optimization that critically influence achievable performance of such energy storage nanostructures.

METHODS

Template preparation starts with electropolishing high purity 99.99% Alfa-Aesar Al sheets. BAA-free templates were fabricated following a two-step anodization procedure in 0.3 M oxalic acid at 40 V. BAA−AAO templates were fabricated by etching the porous membrane formed after first anodization, followed by the formation of a nonporous oxide, or BAA film, in a 2:1 KOH/oxalic acid electrolytic solution. A subsequent anodization in oxalic acid created the ordered template. Templates were highly ordered, with hexagonally spaced pores ($D_{int} \approx$ 100 nm and $D_p \approx$ 40 nm), resulting in pore densities of ~1.15×10^{10} pores/cm^2. Initial pore diameters were widened to $D_p \approx$ 80 nm in a 1:1 $NH_4OH:H_2O$ solution.

For 35BAA-1 μm-p, 35BAA-1.5 μm-p, and 35BAA-2 μm-p, a TiN passivation layer was deposited in a BENEQ TFA 500 commercial reactor. The chamber was held at 175 °C, while the tetrakis (dimethylamido) titanium (TDMAT) precursor as kept at 34 °C and the NH_3 precursor was maintained at 25 °C. Forty cycles were deposited at a rate of ~0.1 nm/cycle, in line with reported values.[37] For all samples, MIM layers were deposited in the same reactor. The chamber was set to 150 °C and all precursors were maintained at 25 °C. The top and bottom electrode were made from Al-doped ZnO (AZO). The bottom electrode was deposited by alternating 1 Al_2O_3 cycle (trimethyl aluminum (TMA) and H_2O precursors) after 10 ZnO cycles (diethyl zinc (DEZ) and H_2O precursors) five times. This provided a target thickness of 10.5 nm AZO, given that the growth rates of an Al_2O_3 and ZnO cycle are ~0.1 and ~0.2 nm/cycle, respectively.[20] Eighty cycles of Al_2O_3 deposited the 8 nm insulator layer. The 102.5 nm top electrode was deposited by alternating 1 Al_2O_3 cycle to 20 ZnO cycles 25 times.

Conventional lithography techniques patterned the 250 μm diameter electrode pads, which wires more than 5 million nanocapacitors in parallel per microcapacitor device (see Supporting Information.). Capacitance was measured with an Agilent 4980A LCR meter at 20 Hz applying 100 mV (AC). Current−voltage (IV) measurement sweeps were measured with a HP 4145B for determining leakage currents and breakdown fields. Analytic SEM was performed with a Hitachi SU-70.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Equations and schematics for calculating area enhancement factor (AEF) and effective planar capacitance (EPC). Figure plotting pore density and area per nanopore as a function of interpore spacing. Histogram of breakdown fields. Explanation and equations for determining nanocapacitor mass. Schematics representing overview of experimental setup. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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